TrueTime

Model 560-5209
56K IRIG-B SYNCHRONIZED GENERATOR

SECTION ONE

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SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5209 card functions as a synchronized generator and provides the user six precision AM, TTL, or RS-422 time code outputs in a Model 56000 chassis. When the 560-5209 card is configured in AM output mode, a variable amplifier (front panel control) connects to six analog output buffers that can drive 50 ohm loads. In TTL output mode IRIG-B DC connects to six digital buffers that can drive 50 ohms. Setting the 560-5209 in RS-422 output mode connects IRIG-B DC to six RS-422 transmitters that can drive 100 ohms. The six outputs connect through the backplane connector and are delivered to external cables via the I/O card installed in the rear slot directly behind the 560-5209 card. In addition to the six outputs, an IRIG-B AM or DC signal can be applied to one of eight user-selected backplane timing bus lines to provide time code for other distribution timing cards in the chassis.

The time code signal source for the card is one of the timing signals that is distributed via INPUT 1 through INPUT 8 on the Model 56000 backplane. The generator decodes and phase locks to the timing input source. The card is configured at installation by DIP switches to select the signal that will be the Primary and Secondary input. The internal oscillator is disciplined to remove any frequency offset with respect to the external reference. This is necessary to maintain precise phase lock and to minimize drift error during periods when all input references are lost.

The Primary and Secondary timing inputs are monitored for activity and code integrity. The activity on both inputs is compared to the delay switch time-out setting (user settable DIP switch) which operates as a watch dog timer. If activity on either the Primary or the Secondary timing inputs exceeds the delay switch time-out setting, that input is considered bad. An input may also be considered “bad” if the minimum input voltage level is not met or if a time code error is detected.

Frequencies of 1, 5 or 10 MHz can be inserted on the Reference Bus inputs A, B, and C to provide a holdover reference source if time code signals are lost from both Primary and Secondary inputs. If this condition exists the internal oscillator will phase-lock to the selected Reference Bus signal.

Note: This card is designed to operate with IRIG-B timing inputs. Since the 560-5209 cannot decode time via a reference bus input, a time code source must be available long enough to be read by the local microprocessor and allow a phase-locked condition to occur.

After phase-lock occurs, time will continue to increment even after the time code input is disconnected.

1.2 FAULT LINE TRANSCEIVER FUNCTION

This is a serial half-duplex signaling operation between the 560-5209 card and the Fault Monitor CPU via the active-low FAULT signal line. The Fault Monitor CPU sends control and switching information to the 560-5209 assembly serially. The 560-5209 assembly provides status information serially to the Fault Monitor CPU.

1.3 PRIMARY/ SECONDARY SIGNAL SELECT FUNCTIONS

If the 560-5209 is operating using the Primary timing input signal and it detects inactivity on this input, the 560-5209 card will automatically or, under Fault Monitor CPU control, switch to the Secondary input signal. If the 560-5209 card is operating in a system with a Fault Monitor CPU card and the 560-5209 card has switched to the Secondary input source, the 560-5209 card will NOT switch back to the Primary input unless commanded by the user via the Fault Monitor CPU.

1.4 PHYSICAL SPECIFICATIONS

Dimensions:	0.8”w X 3.94”h X 8.66”d (2 cm X 10 cm X 22 cm)
Weight:	Approximately ½ pound (¼ kg)

1.5 ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Altitude:	10,000 ft. ASL

1.6 POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	4 W (all six outputs driving 50 ohm loads)

1.7 FUNCTIONAL SPECIFICATIONS

1.7.1 INPUTS

1.7.1.1 Amplitude Modulated Time Code

Format:	AM IRIG-B122
Amplitude:	1 to 5 Vpp
Impedance:	10K Ω to ground
Ratio:	2:1 to 5:1
Error Bypass:	3 frames
Phase Accuracy:	Typically <2 µs

1.7.1.2 DC-Shift Reference Code Input:

Format:	DC-shift IRIG-B002
Levels:	TTL:4K Ω minimum
Error Bypass:	3 frames
Phase Accuracy:	<1µs

1.7.1.3 Reference Bus Inputs REFA, REFB, REFC

Function:	REFA-- Primary External Disciplining Reference for Oscillator REFB-- Secondary External Disciplining Reference for Oscillator REFC-- Tertiary External Disciplining Reference for Oscillator
Input Amplitude:	2-5 Vpp
Input Frequency:	1, 5, or 10 MHz

1.7.2 ANALOG OUTPUTS

Quantity:	6 (plus 1 to timing bus)
Signal Type:	Analog
Amplitude:	0 to 3 Vpp into 50 ohms, adjustable
Signal Delay:	< 350 ns

1.7.3 TTL OUTPUTS (SWITCH SELECTABLE)

Quantity:	6 (plus 1 to timing bus)
Signal Type:	TTL-level
Amplitude:	> 3 Vpk into 50 ohms
Signal Delay:	< 60 ns

1.7.4 RS-422 OUTPUTS (SWITCH SELECTABLE)

Quantity:	6 pairs (plus 1 single to timing bus)
Signal Type:	Differential, centered at 2.5 VDC
Amplitude:	> 2.8 Vpp into 100 ohms
Signal Delay:	< 60 ns
Output Drive Compliance:	
	MIL-STD-188-114A TYPE II BALANCED RS-422-A

1.7.5 DRC CARD COMPATIBILITY

Location:	Slots 1-16 with compatible I/O card in rear slot.
Compatibility:	See Card Compatibility Matrix.

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

Typically, adjacent-card hot swapping has a negligible effect on the 560-5209 card. The effect of redundant power supply switch-over is also negligible.

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5209 analog output card involves selection of the following DIP switches:

1. Primary input signal switch	(SW1-1 TO -8)
2. Secondary input signal switch	(SW2-1 TO -8)
3. Analog driver output switches	(SW3-1 TO -6)
4. Analog timing bus output enable	(SW3-7)
5. Digital / analog output mode switch	(SW3-8)
6. Digital driver output switches	(SW4-1 TO -6)
7. Digital timing bus output enable	(SW4-7)
8. RS-422 / TTL mode switch	(SW4-8)
9. Timing Input Bus Insertion Switch	(SW5-1 TO -8)
10. Primary input enable switch	(SW6-1 TO -4)
11. Secondary input enable switch	(SW7-1 TO -4)
12. Delay switch (activity time-out)	(SW8-1 TO -3)
14. Green status LED enable switch	(SW8-4)
15. Time Quality Output Selects	(SW8-5 TO -6) Not Implemented

16. Input Frequency Division Select (SW8-7 TO -8)
17. Test Reset Switch (Not Installed) (SW9-1)
18. Time Quality Input Selects (SW10-2 TO -3)
    Not Implemented
19. AM/DC Input Mode Select (SW10-1 and SW10-4)

2.3.1 560-5209 REQUIRED MODE SETTINGS

The 560-5209 can operate in one of three output modes. Each mode requires a unique pattern of switch settings. The modes are AM output mode, DC shift RS-422 output mode and DC shift TTL output mode.

2.3.1.1 AM OUTPUT MODE CONFIGURATION

This mode will provide the user with six IRIG-B AM outputs and will enable an additional IRIG-B AM output that may be inserted on the chassis' timing bus. For IRIG-B AM outputs, SW3 and SW4 MUST be set as follows:

SW3 switches 1 through 8 ON
SW4 switches 1 through 8 OFF

2.3.1.2 DC SHIFT RS-422 OUTPUT MODE

This mode will provide the user with six IRIG-B DC shift RS-422 outputs and will enable an IRIG-B DC shift TTL output that may be inserted on the chassis' timing bus. For IRIG-B RS-422 outputs, SW3 and SW4 must be set as follows:

SW3 switches 1 through 8 OFF.
SW4 switches 1-7 ON and switch 8 OFF.

2.3.1.3 DC SHIFT TTL OUTPUT MODE

This mode will provide the user with six IRIG-B DC shift TTL outputs and will enable an additional IRIG-B DC shift TTL output that may be inserted on the chassis' timing bus. For IRIG-B TTL outputs, SW3 and SW4 must be set as follows:

SW3 switches 1 through 8 OFF.
SW4 switches 1-7 ON and switch 8 OFF

2.3.1.3 AM/DC INPUT MODE SELECT

This mode will select demodulator output for AM IRIG-B input or allow DC IRIG-B to pass directly to the processor when high. SW10-1 and -4 must be set as follows:

SW10-1 and -4 ON for DC and OFF for AM

2.3.2 PRIMARY CODE INPUT SOURCE SWITCH (SW1)

Set only one SW1 switch to the ON position. The SW1 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.3 SECONDARY CODE INPUT SOURCE SWITCH (SW2)

Set only one SW2 switch to the ON position. The SW2 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.4 PRIMARY INPUT ENABLE SWITCH (SW6)

This switch MUST be set to a binary representation of the SW1 setting, the Primary input signal switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

PRIMARY INPUT	SW6-1	SW6-2	SW6-3	SW6-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Primary input. If SW6 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Primary input.

2.3.5 SECONDARY INPUT ENABLE SWITCH (SW7)

This switch MUST be set to a binary representation of the SW2 setting, the Secondary input signal switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

SECONDARY INPUT	SW7-1	SW7-2	SW7-3	SW7-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Secondary input. If SW7 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Secondary input.

2.3.6 DELAY SWITCH (Activity Time-Out SW8 Switches 1, 2, & 3)

SW8 switches 1 through 3 are used to set the input activity time-out delay. The user should set the delay for a time-out value that is the closest to, but longer than, the period of the input signal. (Input must have an amplitude higher than 1.8 Vpp.) This will provide fault detection in the shortest amount of time (Primary to Secondary switch-over time is minimized).

Example Setting: If the input signal is IRIG-B AM (10 milliseconds between the beginning of each BCD bit), the appropriate setting would be SW8-1 OFF, SW8-2 ON, SW8-3 OFF (20.48 millisecond time-out).

The delay switches could be set for IRIG-B exclusively; but different settings are made available for future upgrades that would include time codes other than IRIG-B. These other time codes could have different bit rates that would require switch delays other than 20.48 milliseconds.

DELAY (TIME-OUT)	SW8-1	SW8-2	SW8-3
204.8 microseconds	OFF	OFF	OFF
2.048 milliseconds	ON	OFF	OFF
20.48 milliseconds	OFF	ON	OFF
204.8 milliseconds	ON	ON	OFF
2.048 seconds	OFF	OFF	ON
20.48 seconds	ON	OFF	ON
122.88 seconds	OFF	ON	ON
Infinite	ON	ON	ON

If infinite delay has been selected, Primary and Secondary input fault detection is disabled.

2.3.7 GREEN LOCK LED ENABLE (SW8-4)

The indication of the synchronized generator being in a phase-locked state can be indicated two ways. One option is to indicate phase-lock by illuminating the green/red input status LED to a green state. This is done by setting SW8-4 to the ON position. If SW8-4 is set to the OFF position, a phase-locked condition will be indicated by turning the green LED off. (Lock will be indicated by the fault LED OFF.)

GREEN LOCK LED	SW8-4
Green LED OFF if Locked	OFF
Green LED ON if Locked	ON

2.3.8 TIMING INPUT BUS INSERTION SWITCH (SW5)

Set <u>one</u> SW5 switch to the ON position. This switch-bank selects which one of the eight possible chassis timing inputs will receive the 560-5209's generated time code signal. The SW5 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane. If the user desires *not* to insert time code on the bus, all SW5 switches should be set to OFF.

2.3.9 EXTERNAL REFERENCE ENABLE (SW8)

Set SW8 switches 7 and 8 to select the correct frequency from the Reference Input Bus.

SELECTED FREQ	SW8-7	SW8-8
Disabled	ON	ON
1 MHz	OFF	OFF
5 MHz	OFF	ON
10 MHz	ON	OFF

2.4 FAULT STATUS INDICATIONS

All LED indicators activate briefly following hot-insertion or power-up. The following paragraphs describe operation during steady-state conditions.

2.4.1 INPUT SIGNAL STATUS INDICATOR

The P/S indicator provides a visual indication of Primary and Secondary signal loss and phase-lock. The various status indications are described below:

Blinking Red	Loss of Signal
Solid Red	Local Power Supply Failure.
Solid Amber	Code Error
Solid Green	Code OK (if SW8-4 = ON)
Off	Phase Locked (if SW8-4 = OFF)

2.4.2 OUT FAULT INDICATORS

The OUT A through OUT F fault indicators activate when the associated output drivers have failed. Note that the detector is designed to detect failed drivers and may not detect a shorted output.

2.4.3 INIT. FAULT INDICATOR

This is an on-card fault indicator, which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.4.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5209 card status. This status is available via the Fault Monitor CPU serial port. When it is presented in a 2-byte format, with individual bit definitions as follows:

FAULT STATUS 0	BIT	STATUS (1 = ACTIVE)
Low	0	Output Fault A*
Nibble	1	Output Fault B*
Low	2	Output Fault C*
Byte	3	Output Fault D*
High	4	Output Fault E*
Nibble	5	Output Fault F*
Low	7	Code Error[1]
FAULT STATUS 1	**BIT**	**STATUS (1=ACTIVE)**
Low	0	Power Cycled
Nibble	1	Primary Input Inactive*
High	2	Secondary Input Inactive*
Byte	3	Source = Primary
High	4	Not Defined
Nibble	5	Not Defined
High	6	Not Defined
Byte	7	Not Defined

STATUS REG 0	BIT	STATUS (1=ACTIVE)
Low	0	Pri Input Enable SW6-1
Nibble	1	Pri Input Enable SW6-2
Low	2	Pri Input Enable SW6-3
Byte	3	Pri Input Enable SW6-4
High	4	Sec Input Enable SW7-1
Nibble	5	Sec Input Enable SW7-2
Low	6	Sec Input Enable SW7-3
Byte	7	Sec Input Enable SW7-4
STATUS REG 1	**BIT**	**STATUS (1=ACTIVE)**
Low	0	Delay SW8-1
Nibble	1	Delay SW8-2
High	2	Delay SW8-3
Byte	3	Green LED Enabled SW8-4
High	4	Time Quality Out 1 SW-5[2]
Nibble	5	Time Quality Out 2 SW-6[2]
High	6	Input Frequency 0 SW8-7
Byte	7	Input Frequency 1 SW8-8
STATUS REG 2	**BIT**	**STATUS (1=ACTIVE)**
Low	0	Analog Outputs SW3-8
Nibble	1	TTL Outputs SW4-8
Low	2	DC Mode SW10-4
Byte	3	Input Quality 2 SW10-1[2]
High	4	Input Quality 2 SW10-2[2]
Nibble	5	Input Quality 2 SW10-3[2]
Low	6	Not Defined
Byte	7	Not Defined

* Latched fault bit--reset via Fault Monitor CPU.
[1] Bit set when bit errors are detected in IRIG-B.
[2] These controls are not implemented at this time.

560-5209 CARD ID: 0x1070

2.5 SYNCHRONIZED GENERATOR OPERATION

By definition, a time code synchronized generator is an instrument that decodes a time code input and produces a time code output. This signal is synchronized to the time code input signal. If the input signal is lost, the output code will continue to increment at a calculated rate. This rate is at least ten times more accurate than the signal would be if it were free-running.

2.5.1 OPERATION FROM POWER-UP TO PHASE-LOCK

When the 560-5209 chassis is first powered up, a sequence of events will begin to occur. The switch-selected time code source will be the first signal source to the decoding section of the unit. It will take approximately 13 seconds for the time code to be decoded. Once the input code has been decoded, the synchronized generator will begin to output the correct time plus or minus half of a second. During the following second, the front panel P/S LED will illuminate to amber, indicating that the internal oscillator is phase-locking to the input source. The exact amount of time that it takes for a phase locked condition to occur depends on the accuracy of the time code source compared to the accuracy or the internal oscillator. Once phase lock occurs, the front panel P/S LED will turn green (if SW4-8 is ON). When locked, the time code output should be on-time (with respect to the input) ±2 microseconds in AM input mode or ±1 microsecond in 422 or TTL mode.

If both primary and secondary IRIG-B input sources are lost and one or more frequency reference sources are available on the FREQA, FREQB, and/or FREQC inputs, these will be used to phase lock until the IRIG-B input is re-established. The frequency reference inputs are automatically selected as follows:

If FREQA, then FREQA.
If not FREQA, then FREQB.
If not FREQA and not FREQB, then FREQC.
If FREQA or FREQB return, then they are used.

These frequency inputs can be 1, 5, or 10 MHz.

2.5.2 CODE ERRORS

If a code error is present for more than 3 frames of code (3 seconds for IRIG-B), a code error condition will cause a fault switch to the next available input source.

2.5.3 AM OUTPUT LEVEL ADJUSTMENT

The 560-5209 AM output mode allows the user to adjust the AM output (via the front-panel-accessible potentiometer) over a range of 0 to 3.8 volts peak to peak (50 Ω load) or ~7 Vpp (no load).

2.5.4 TIME QUALITY DATA

Various TrueTime products generate and handle time quality data that is included in the incoming and/or the outgoing IRIG-B time code. The 560-5209 will simply “copy” the incoming time quality data to the generated IRIG-B time code. This allows the time

quality data to be passed from upstream to downstream timing equipment.

SECTION THREE

3 THEORY OF OPERATION

3.1 ACTIVITY DETECTION

All time code and frequency input signals are converted to CMOS levels. The resultant digital signal is connected to and analyzed by the FPGA for activity to determine if a given input signal is present.

3.2 DECODING CIRCUIT

AM IRIG-B input levels are regulated to a known peak to peak voltage levels by an automatic gain control (AGC) circuit. The output of the AGC is connected to both a carrier detector and a mark detector. The detected mark and carrier are processed by the FPGA which in turn produces digital code that is connected to, read by and translated by the microprocessor.

DC input code is also translated by the microprocessor. However, the decoding circuitry involved in translating AM code proceeding the microprocessor is completely bypassed.

3.3 TIME CODE GENERATION

The translated code that is read by the microprocessor will be regenerated based on the internal temperature controlled oscillator, which is also utilized as a processor clock. The input code frame and the generated code frame are compared to each other at the first rising edge of each new frame. The microprocessor uses this comparison to “steer” the internal oscillator by varying its control voltage through a digital to analog converter.

3.3.1 DC CODE GENERATION AND DISTRIBUTION

The time code generated by the microprocessor is actually IRIG-B DC. This digital code is connected to the FPGA which internally distributes it to seven FPGA outputs. The seven FPGA outputs are individually buffered by unity-gain differential amplifiers. Six of the differential pairs are available for distribution in RS-422 mode to any Model 56000 differential output interface module. In TTL mode the non-inverted outputs are double-buffered for driving 50 ohm loads via a BNC output interface module. A seventh TTL output is available for insertion on the timing bus via a user selected switch.

3.3.2 AM CODE GENERATION AND DISTRIBUTION

In time with the generated IRIG-B DC, the microprocessor generates a 1 KHz signal. This signal is connected to a squarewave to sinewave converter to produce a 1 KHz sinewave which is modulated by the generated IRIG-B DC to produce IRIG-B AM. This AM code is connected to seven analog buffers of which six are made available for distribution via a BNC output interface module. The seventh output is available to be inserted on the timing bus via a user switch selection.

3.4 OUTPUT ACTIVITY DETECTION

When switch-selected, each of the six IRIG-B AM outputs are connected to an individual comparitor which sends TTL levels that can be activity detected by the FPGA. For both DC modes, the non-inverted outputs can be switch selected to connect to the same comparitors for activity detection. The inverted outputs are directly connected to the FPGA to process activity detection.

3.5 FIELD PROGRAMMABLE GATE ARRAY (FPGA)

The main function of the FPGA is to process status information that is transmitted to and received from the CPU Fault Monitor Module.

SECTION FOUR

4.0 DETAILED DRAWINGS

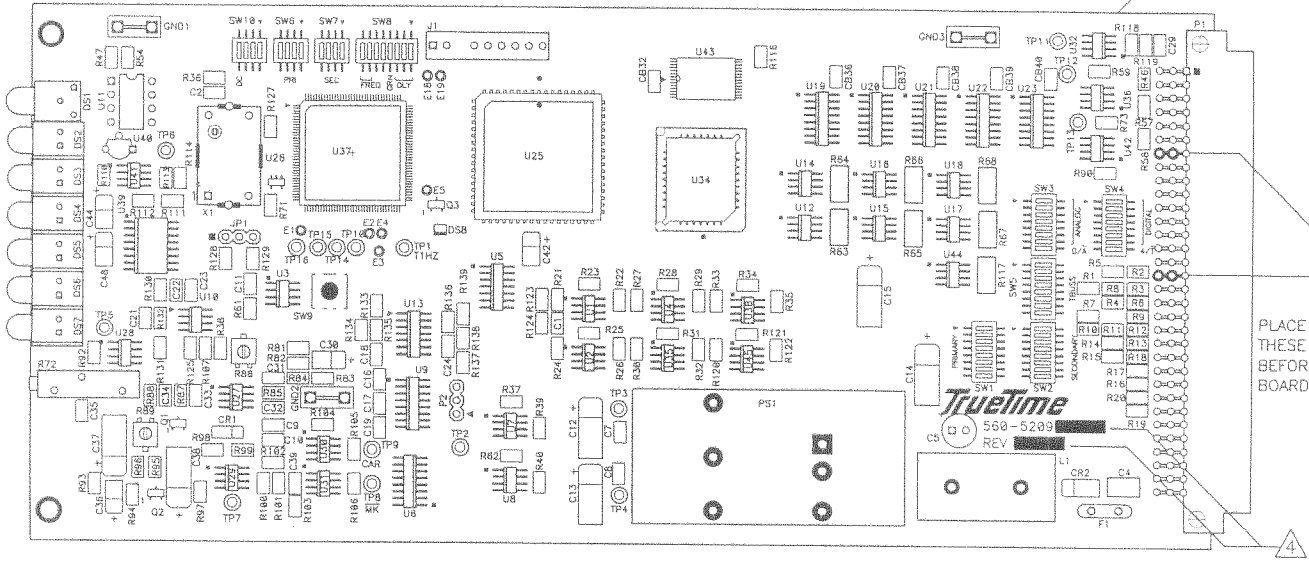
4.1 560-5209 BILL OF MATERIALS / ASSEMBLY DRAWINGS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER ASSEMBLY REQUIREMENTS DOCUMENT 421-11.
2. RESISTOR VALUES IN OHMS, CAPACITORS IN MICRO FARADS.
3. POLARIZED CAPACITORS ARE SHOWN WITH A ROUNDED EDGE INDICATING THE POSITIVE SIDE.
4. STAMP DASH NUMBER AND REVISION LEVEL.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
02	MODIFIED DESIGN	04/28/99	
03	MODIFIED DESIGN	09/08/99	



CONTRACT NO.		
APPROVALS		DATE
DRAWN BY	B.A.S.	01-29-99
CHECKED		
APPROVED		

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Title	TIME CODE SYNC GEN ASSEMBLY DRAWING, TOP SIDE	
Size	Number	Rev
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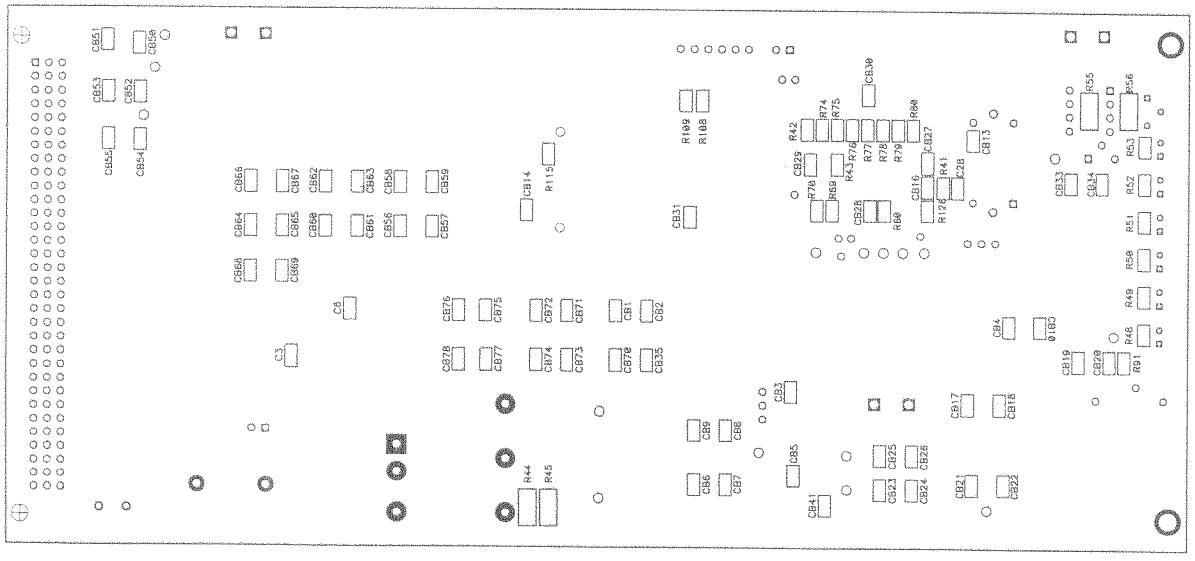
Date Fri Sep 10, 1999 13:19:29		
File name 2209-03.PCB		Sheet 1 of 9



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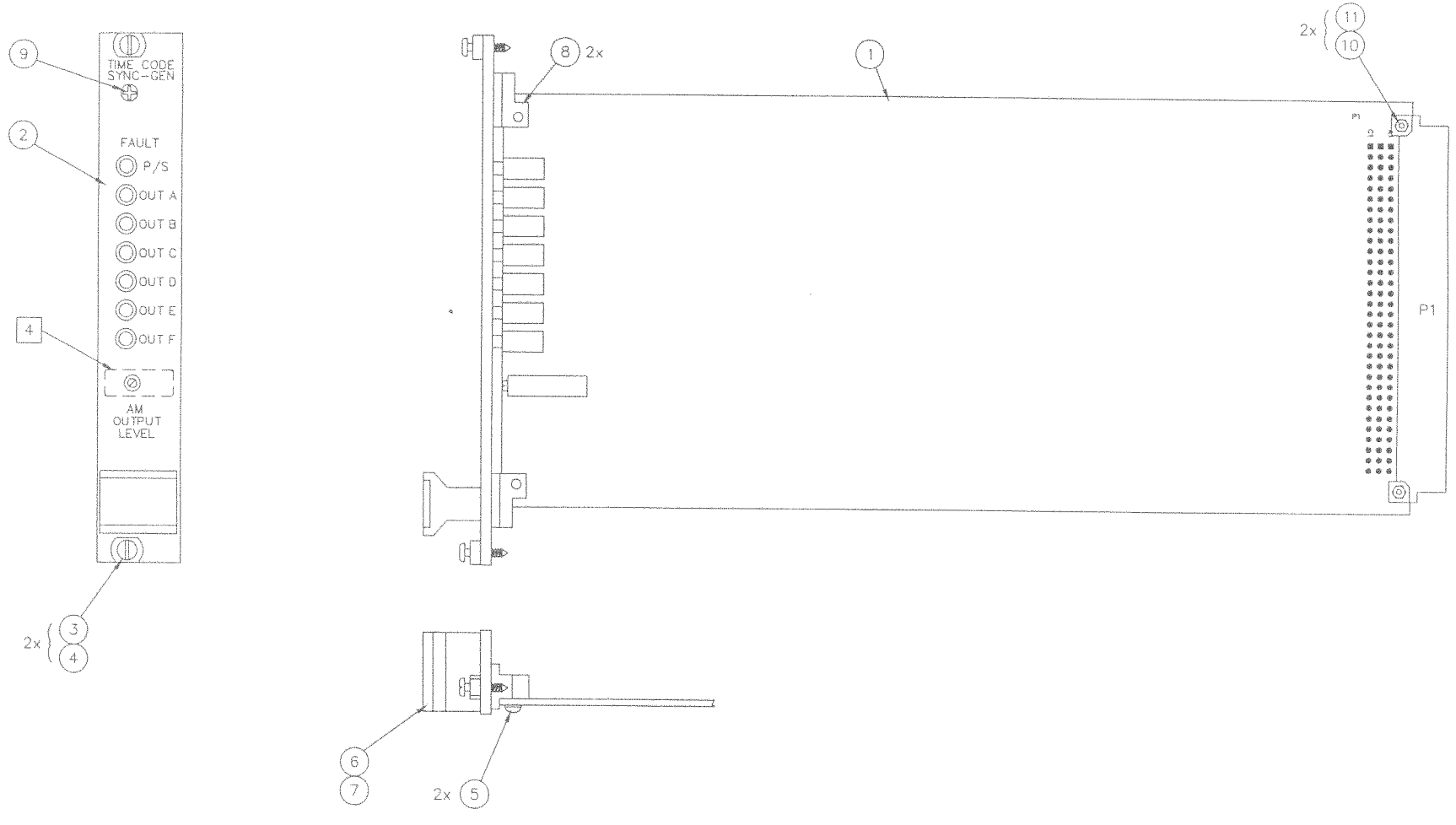
Title	TIME CODE SYNC GEN ASSEMBLY DRAWING, BOTTOM SIDE	
Size: B	Number: 560-5209	Rev: 03
Date: Fri Sep 10, 1999 13:38:14		
Filename: 2209-03.PCB		Sheet 2 of 9



4 REFER TO CARD DASH NUMBER FOR APPROPRIATE LABEL. LABEL ATTACHED AT FINAL TEST.

NOTES: (CONT'D)

FILENAME: \560\5209
DATE: 09-10-99

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SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		560-5209	03

SCALE NONE

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
560-5209	ASSY SYNC GEN	MADE FROM 560-2209				EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		9-99
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV 03 (09-10-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		560-5209 REV 03
0000-REV	PCB REV LEVEL HERE >>>>		000000		1.0000	EA		560-2209 REV 03
003S-1000	RES 2010 100 OHM 1% 1/2W	CAL-CHIP RM20F1000CT(NAV)	000000		2.0000	EA		R44,45
003S-39R0	RES 2010 39 OHM 5% 1/2W	CAL-CHIP RM20J390CT (NAV)	000000		7.0000	EA		R63-68,117
003S-6801	RES 2010 6.8K OHM 5% 1/2W	CAL-CHIP RM20J682CT (NAV)	000000		2.0000	EA		R55,56
008S-100	RES 0805 10 OHM 5% 1/8W	CAL-CHIP RM10J100CT (NAV)	000000		1.0000	EA		R71
008S-1000	RES 0805 100 OHM 1% 1/8W	CAL-CHIP RM10F1000CT(NAV)	000000		1.0000	EA		R129
008S-1002	RES 0805 10K OHM 1% 1/8W	CAL-CHIP RM10F1002CT(NAV)	000000		4.0000	EA		R92,93,95,119
008S-101	RES 0805 100 OHM 5% 1/8W	CAL-CHIP RM10J101CT (NAV)	000000		1.0000	EA		R126
008S-102	RES 0805 1K OHM 1% 1/8W	CAL-CHIP RM10F1001CT(NAV)	000000		20.0000	EA		
	R22,26,29,32,35,36,38,39,40,42,46,57,58,122,124,133,134,136,137,139							
008S-1022	RES 0805 10.2KOHM 1% 1/8W	CAL-CHIP RM10F1022CT(NAV)	000000		3.0000	EA		R84,85,87
008S-103	RES 0805 10K OHM 5% 1/8W	CAL-CHIP RM10J103CT (NAV)	000000		3.0000	EA		R111,131,132
008S-104	RES 0805 100K OHM 1% 1/8W	CAL-CHIP RM10F1003CT(NAV)	000000		6.0000	EA		R41,59,73,90,113,118
008S-105	RES 0805 1M 5% 1/8W	CAL-CHIP RM10J105CT (NAV)	000000		2.0000	EA		R125,130
008S-152	RES 0805 1.5K OHM 5% 1/8W	CAL-CHIP RM10J152CT (NAV)	000000		1.0000	EA		R101
008S-153	RES 0805 15K OHM 5% 1/8W	CAL-CHIP RM10J153CT (NAV)	000000		1.0000	EA		R102
008S-154	RES 0805 150K OHM 5% 1/8W	CAL-CHIP RM10J154CT (NAV)	000000		3.0000	EA		R94,104,114
008S-202	RES 0805 2K OHM 5% 1/8W	CAL-CHIP RM10J202CT (NAV)	000000		1.0000	EA		R110
008S-222	RES 0805 2.2K OHM 5% 1/8W	CAL-CHIP RM10J222CT (NAV)	000000		27.0000	EA		
	R1-19,21,24,27,30,33,91,100,120							
008S-225	RES 0805 2.2M OHM 5% 1/8W	CAL-CHIP RM10J225CT (NAV)	000000		1.0000	EA		R96
008S-302	RES 0805 3K OHM 5% 1/8W	CAL-CHIP RM10J302CT (NAV)	000000		2.0000	EA		R99,103
008S-332	RES 0805 3.3K OHM 5% 1/8W	CAL-CHIP RM10J332CT (NAV)	000000		2.0000	EA		R135,138
008S-391	RES 0805 392 OHM 1% 1/8W	CAL-CHIP RM10F3920CT(NAV)	000000		1.0000	EA		R97
008S-471	RES 0805 470 OHM 5% 1/8W	CAL-CHIP RM10J471CT (NAV)	000000		11.0000	EA		R47-54,81-83
008S-472	RES 0805 4.7K OHM 5% 1/8W	CAL-CHIP RM10J472CT (NAV)	000000		21.0000	EA		
	R43,60,69,70,74-80,88,105,106,108,109,115,116,123,127,128							
008S-473	RES 0805 47K OHM 5% 1/8W	CAL-CHIP RM10J473CT (NAV)	000000		3.0000	EA		R20,61,107
008S-4753	RES 0805 475K OHM 1% 1/8W	CAL-CHIP RM10F4753CT(NAV)	000000		8.0000	EA		
	R23,25,28,31,34,37,62,121							
008S-753	RES 0805 75K OHM 5% 1/8W	CAL-CHIP RM10J753CT (NAV)	000000		1.0000	EA		R98
008S-822	RES 0805 8.2K OHM 5% 1/8W	CAL-CHIP RM10J822CT (NAV)	000000		1.0000	EA		R112
019-002	POT 5K 20 TURN	BECKMAN 89PR5K	000000		1.0000	EA		R72
019S-001	POT, SNGL TURN SEALED 5K	BOURNS 3314G-1-502E (SMD)	000000		1.0000	EA		R89
019S-003	POT, SNGL TURN SEALED 20K	BOURNS 3314G-1-203E (SMD)	000000		1.0000	EA		R86
023-010-100	CAP AE 10UF 100V R	PANASONIC ECE-A2AU100	000000		1.0000	EA		C5
036S-NP0101	CAP 100PF NPO 100V 0805	NIC NMC0805NP0101J100TR	000000		3.0000	EA		C24,35,39
036S-NP0102	CAP .001UF NPO 100V 0805	NIC NMC0805NP0102J100TR	000000		6.0000	EA		C3,6-10

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
036S-X7R.0047	CAP .0047UF X7R 0805 10%	CALCHIP GMC21X7R472K50NT	000000		2.0000	EA		C32,33
036S-X7R103	CAP .01UF X7R 50V 0805	NIC NMC0805X7R103K50TR	000000		1.0000	EA		C22
036S-X7R104	CAP .1UF X7R 100V 1210	NMC1210X7R104K100TR (NAV)	000000		1.0000	EA		C4
036S-X7R104-50	CAP .1UF X7R 50V 0805 10%	NIC NMC0805X7R104K50TR	000000		73.0000	EA		
	C1,2,11,21,23,28,29; CB1,CB2,CB4-CB10,CB13,CB14,CB16-CB41,CB50-CB78							
036S-X7R473-50	CAP .047UF X7R 50V 0805	NIC NMC0805X7R473K50TR	000000		2.0000	EA		C31,34
037S-106	CAP 10UF 25V 7343 10%	NIC NTC-T106K25TRD (NAV)	000000		1.0000	EA		C38
037S-225	CAP 2.2UF 16V 3528	NIC NTC-T225K16TRB	000000		5.0000	EA		C30,36,42,44,48
037S-686	CAP 68UF 6.3V 7343	NTC-T686K10TRD-BOM NAV	000000		5.0000	EA		C12-15,37
041-000	FERRITE BEAD	FAIR-RITE 2661000101	000000		4.0000	EA		12
045-33	INDUCTOR 33UH 5.5A	DALE IHM-2 33UH +/-10%	000000		1.0000	EA		L1
057S-4002	DIODE 4002	ROHM RLR4002	000000		1.0000	EA		CR2
057S-4148	DIODE 1N4148	ROHM RLS4148TR	000000		1.0000	EA		CR1
058-020	LED	DIALIGHT 550-3007	000000		6.0000	EA		DS2-7
058-027	LED RED/GREEN	DIALIGHT 550-3505	000000		1.0000	EA		DS1
058S-001	LED RED X SML W RES SFMT	HP HLMP-6600-G0012	000000		1.0000	EA		DS8
065S-004	SWITCH DIP HALF PITCH	AUGAT/THOM&BETTS GDH04S	000000		3.0000	EA		SW6,7,10
065S-005	SWITCH DIP 8 HALF PITCH	AUGAT GDH08S	000000		6.0000	EA		SW1-5,8
174S-XC5204T	XILINX XC5204T FPGA	XILINX XC5204-6TQ144C	000000		1.0000	EA		U37
175S-2N2907A	TRANSISTOR 2N2907A SOT-23	MOTOROLA MMBT2907AL	000000		1.0000	EA		Q3
175S-J177	TRANSISTOR J177 SOT-23	MOTOROLA MMBFJ177L	000000		2.0000	EA		Q1,2
176-431	TL431CLP REGULATOR/3 PIN	TEXAS INST TL431CLP	000000		1.0000	EA		U40
176-68HC11F1	IC, CPU	MOTOROLA MC68HC11F1CFN3	000000		1.0000	EA		U25
176-LH1512	1 NC 1 NO SSR	SIEMENS LH1512AB	000000		1.0000	EA		U11
176S-26C31	QUAD 422 LINE DRIVER	NSC DS26C31TM	000000		5.0000	EA		U19-23
176S-29C512-12	FLASH EPROM 64KX8 32PLCC	ATMEL AT29C512-12JC	000000		1.0000	EA		U34
176S-BUF634U	HIGH SPEED BUFFER	BURR-BROWN BUF634U (SO8)	000000		7.0000	EA		U12,14-18,44
176S-LM311M	VOLTAGE COMPARATOR	NATL LM311M (8SOIC)	000000		10.0000	EA		
	U1,2,4,7,8,30,31,35,38,45							
176S-LM339	QUAD COMPARATOR LM339	NATL LM339M	000000		1.0000	EA		U13
176S-LT1016	LT1016 (8SO)	LINEAR TECH LT1016CS8	000000		3.0000	EA		U32,36,42
176S-MC34064	UNDER VOLTAGE SENSING CKT	MC34064DM (SEE BOM NAV)	000000		1.0000	EA		U3
176S-PCM56U	DIGITAL-ANALOG CONVERTER	BURR-BROWN PCM56U	000000		1.0000	EA		U39
176S-TL082	J-FET INPUT OP AMP (8SO)	TI TL082BCD	000000		3.0000	EA		U27-29
178S-74AHC1GU04	SINGLE UNBUFFERED INVERTR	TI SN74AHC1GU04DBVR	000000		1.0000	EA		U26
178S-74HC00	74HC00 (14SO)	RCA CD74HC00M	000000		1.0000	EA		U5
178S-HC4053D	ANALOG MUX, 2CHX3	MOT MC74HC4053D (NARROW)	000000		1.0000	EA		U6
178S-IS62C256	STATIC RAM 32KX8(28TSOP)	ISSI IS62C256-70TI	000000		1.0000	EA		U43
178S-TLC272	TLC272 (8SO)	TI TLC27L2CD	000000		2.0000	EA		U10,41
185-015	PROGRAMMED PROM	FOR 56K SYNC GEN	000000		1.0000	EA		FOR U34
223-138	SCREW SH CH ZN M2.5X10	SCHROFF #21100-138	000000		2.0000	EA		10
223-144	NUT M2.5	SCHROFF 21100-144	000000		2.0000	EA		11
223-181	HOLDER (PB) DIE CAST	SCHROFF 20827-072	000000		2.0000	EA		08
223-295	HANDLE	SCHROFF #20809-295	000000		1.0000	EA		07
223-379	SCREW CAP NP M2.5 X 11	SCHROFF #21100-379	000000		2.0000	EA		03

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
223-464	SLEEVE, STAINLESS	SCHROFF 21100-660	000000		2.0000	EA		04
223-500	SCREW PH FH NP M2.5X10	SCHROFF #21100-500	000000		1.0000	EA		09
249-005	SCREW M2.5 X 8	SCHROFF #21100-140	000000		2.0000	EA		05
249-007	SCREW SH CH ZN M2.5X12	SCHROFF 21100-148	000000		1.0000	EA		06
273-009	TERMINAL TEST POINT	COMP CORP PJ-201-25	000000		3.0000	EA		GND1-3
273-015	TERM TEST POINT (WHITE)	COMP. CORP TP-104-01-09	000000		16.0000	EA		TP1-16
345-050	OSC 10 MHZ TCXO	TOYOCOM TCO-919R-10.0	000000		1.0000	EA		X1
355-BXA10-1	DC-DC 18-75VIN +5/-5 OUT	ARTESYN BXA10-48D05	000000		1.0000	EA		PS1
363-0.9LV	POLYSWITCH 0.9A (60 VOLT)	RAYCHEM RXE090	000000		1.0000	EA		F1
372-96P	CONN,96-P ML DIN RT ANGLE	BERG 70077-027 (BOM NAV)	000000		1.0000	EA		P1
379S-032	SOCKET 32-P PLCC	AMP 822274-1	000000		1.0000	EA		FOR U34
401-01-01-03LP	LO-PROFILE 1X3 PIN HEADER	SWTEC MTLW-103-05-G-S-185	000000		1.0000	EA		P2
401-01-01-34	CONN 36-P HDR SNGL RW W/W	3M 929834-01-36	000000		1.0000	EA		JP1 (CUT TO 3 PINS)
560-1262	PNL,FRT 56K SYNC GEN	FAB/SCREEN	000000		1.0000	EA		02
560-2209	PCB SYNC GEN	FAB	000000		1.0000	EA		01
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
NOTE 1			000000		1.0000	EA		
	NOT INSTALLED: C16-C19, CB3 U9 SW9							
OSV560-5209	OUTSIDE LABOR 560-5209	PCA	000000		1.0000	EA		